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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,692	08/11/2003	HSIANG-LAN LUNG	10156-US-PA	1691
31561 7	7590 12/01/2006		EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE			WARREN, MATTHEW E	
7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2		ART UNIT	PAPER NUMBER	
TAIPEI, 100	-		2815	
TAIWAN	-	•	DATE MAILED: 12/01/200	6

Please find below and/or attached an Office communication concerning this application or proceeding.

		/ \(\rightarrow\)					
	Application No.	Applicant(s)					
	10/604,692	LUNG ET AL.					
Office Action Summary	Examiner	Art Unit	+				
·	Matthew E. Warren	2815					
The MAILING DATE of this communication ap Period for Reply	ppears on the cover sheet with	h the correspondence address					
A SHORTENED STATUTORY PERIOD FOR REPI WHICHEVER IS LONGER, FROM THE MAILING [- Extensions of time may be available under the provisions of 37 CFR 1 after SIX (6) MONTHS from the mailing date of this communication If NO period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by statu Any reply received by the Office later than three months after the maili earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNIC .136(a). In no event, however, may a report of the community of the c	ATION. ply be timely filed HS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).					
Status							
1) Responsive to communication(s) filed on 10.	<u> August 2006</u> .		i				
2a)⊠ This action is FINAL . 2b)□ Th	☐ This action is FINAL . 2b)☐ This action is non-final.						
3) Since this application is in condition for allows	ance except for formal matte	rs, prosecution as to the merits is					
closed in accordance with the practice under	Ex parte Quayle, 1935 C.D.	11, 453 O.G. 213.					
Disposition of Claims							
4) Claim(s) 1,4-6,8-10 and 35-37 is/are pending	4)⊠ Claim(s) <u>1,4-6,8-10 and 35-37</u> is/are pending in the application.						
,	4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1, 4-6, 8-10 and 35-37</u> is/are rejected	ed.						
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/	or election requirement.						
Application Papers							
9) The specification is objected to by the Examir	ner.						
10) The drawing(s) filed on is/are: a) ac		y the Examiner.					
Applicant may not request that any objection to the							
Replacement drawing sheet(s) including the corre							
11) ☐ The oath or declaration is objected to by the E	Examiner. Note the attached	Office Action or form PTO-152.					
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreig a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document	nts have been received. nts have been received in Ap	oplication No					
 Copies of the certified copies of the pri application from the International Bure 		eceived in this National Stage					
* See the attached detailed Office action for a lis		received.					
Attachment(s) 1) Notice of References Cited (PTO-892)	A) Interview S	ummary (PTO-413)					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date					
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	5) Notice of In	formal Patent Application					

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DETAILED ACTION

This Office Action is in response to the Amendment filed August 10, 2006.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6, 8-10 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamigaki et al. (US 6,894,344) in view of Lee et al. (US 6,862,223 B1).

With regards to claims 1 and 35, Kamigaki illustrates in figures 1-114 (entire document), particularly figures 2, a substrate 1; a charge-trapping layer 2-1 and 2-2 on the substrate; a split gate 7-1 on the charge-trapping layer, wherein the split gate is composed of at least two separated conductive pieces and the conductive pieces are shorted with each other (through 5) and are arranged adjacently to form the at least one split region; and including at least one split region directly over the charge-trapping layer; and a source/drain 4-1/4-2 in the substrate beside the split gate. With regards to claim 1, the limitation "the charge-trapping layer around the split region serves as a coding region" is an inherent function of the structure and since the prior art has the same structure and materials as the claimed invention it will have the same inherent function as a memory device. Kamigaki shows all of the elements of the claims except

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the two separated conductive pieces arranged adjacently to form the at least on split region without any other conductor in the split region. Lee et al. shows (fig. 2A-2B) that a memory device comprises gates (SG1 or SG2) having a poly1 and poly2 layer formed adjacent to each other (one above and one below). The gates have a split region and are shorted to each other. There is no other conductor between them in the split region. With this configuration the flatness on the silicon surface is improved. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the split gates of Kamigaki by forming the two shorted gates without a conductor in the split region as taught by Lee to improve the surface flatness of the device.

With regards to claim 4, Kamigaki illustrates in fig. 2 the conductive pieces of the split gate include a pair of conductive spacers 7-1 and a conductive layer 6 between the pair of conductive spacers.

With regards to claim 5, Kamigaki illustrates in fig. 2 the pair of conductive spacers 7-1 are arranged with two substantially vertical sidewalls thereof adjacent to the source/drain 4-l/ 4-2.

With regards to claim 6, Kamigaki illustrates in fig. 2 an insulator (inherent) on the source/drain, wherein the pair of conductive spacers 7-1 are disposed on the sidewalls of the insulator.

With regards to claim 8, Kamigaki illustrates in fig. 2 the conductive pieces 6 and 7-1 are separated from each other by a dielectric layer (inherent).

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With regards to claim 9, Kamigaki discloses in col. 18, lines 39-40, the split gate 6-1 and 6-2 comprises polysilicon.

With regards to claim 10, Kamigaki discloses in col. 6, lines 16-26, the charge-trapping layer comprises a silicon nitride layer disposed between two silicon oxide layers.

With regards to remaining limitations of claim 35, and claims 36-37, the claimed "programming operation" is not considered to add any structure to the claimed device and is considered to be intended use of the device. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Claims 11 and 12 are rejected under 35 USC § 103 (a) as being unpatentable over Kamigaki in view of Lee as applied to claim 1 above, and further in view of Schwabe et al. (US 4,257,832).

With regards to claim 11, Kamigaki and Lee are discussed above, it does not show the charge-trapping layer comprises aluminum oxide (Al₂0₃). Schwabe discloses in col. 3, lines 11-15 a charge- trapping layer comprises aluminum oxide (Al₂0₃). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trapping layer of Kamigaki and Lee by using Al₂0₃ as a tunnel oxide taught by Schwabe to form a suitable charge trapping layer.

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With regards to claim 12, Schwabe illustrates in fig. 5 the substrate comprises a p-substrate 11, and the source/drain comprises an n-type source/drain 14/19. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Response to Arguments

Applicant's arguments with respect to claims 1, 4-6, 8-10 and 35-37 have been considered but are most in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MEW
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November 27, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER